AN INTERMEDIATE STRUCTURE HAVING A SILICON NITRIDE BARRIER LAYER ENCAPSULATING A SEMICONDUCTOR SUBSTRATE

CROSS-REFERENCE TO RELATED APPLICATIONS

A.M 5/17/05 A.M 5/17/05

[0001] This application is a continuation ~~in part~~ of application Serial No. 09/259,145, filed February 26, 1999, ~~abandoned~~, which is a divisional of application Serial No. 08/975,039, filed November 18, 1997, now U.S. Patent 6,069,059, issued May 30, 2000.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The present invention relates to an apparatus and method for forming isolation structures for isolating electrical devices on a semiconductor substrate. More particularly, the present invention relates to forming the isolation structure using a novel LOCOS (LOCal Oxidation of Silicon) technique.

[0003] State of the Art: The fabrication of an electrical circuit involves connecting isolated electrical devices with specific electrical paths. For the sake of example only, the follow discussion will focus on the formation of a twin-well CMOS (Complementary Metal Oxide Semiconductor) structure. In the fabrication of a CMOS integrated circuit, the isolation structure for electrically isolating the electrical devices must be built onto or into the silicon wafer itself. The individual electrical devices are generally isolated using the LOCOS process. FIGs. 14 through 27 illustrate the LOCOS process which begins with a semiconductor substrate 202, such as a silicon wafer, having p-wells 204 and n-wells 206 formed thereon, as shown in FIG. 14. A layer of silicon dioxide 210, usually between about 20 and 50 nm thick is formed on an active surface 208 of the semiconductor substrate 202, as shown in FIG. 15. The silicon dioxide layer 210 may be formed by any known technique, including but not limited to: thermally growing the layer, CVD (chemical vapor deposition), and the like. The function of the silicon dioxide layer 210, also called pad or buffer oxide, is to lessen the stresses between the semiconductor substrate 202 and a subsequently deposited silicon nitride layer.

[0004] As shown in FIG. 16, after the formation of the silicon dioxide layer 210, a thick layer of silicon nitride 212, usually between about 100 and 200 nm thick, is deposited, generally